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Facile Formation of Graphene P–N Junctions Using Self-Assembled Monolayers

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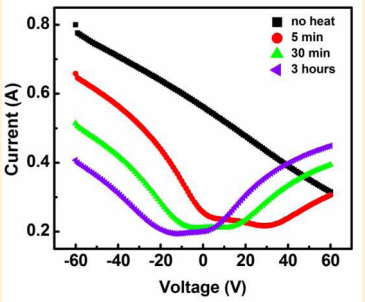
Supporting Information

ABSTRACT: Monolithic and patterned aminopropyltriethoxysilane (APTES) layers are used to create n-doped graphene, graphene p–n junctions, and FET devices containing p–n junctions in the device channel through transfer of CVD graphene onto APTES coated substrates. APTES doping is shown to not result in introduction of defects. *I*–*V* measurements of FET devices containing patterned APTES layers show it is possible to control the position of the two current minima (two Dirac points) in the ambipolar p–n junction.



1. INTRODUCTION

Graphene, a two-dimensional sp^2 hybridized carbon lattice that is also the fundamental building block of graphite, has attracted significant interest recently due to its distinctive electrical and mechanical properties,[1,2] including its nearly linear energy dispersion relation that results in electric field induced generation of electrons and holes which travel as massless Dirac fermions with high velocities.[3−5] Carrier mobilities in pristine graphene have been estimated to be as large as 200 000 $cm^2/(V\ s)$, which is several orders-of-magnitude larger than crystalline silicon and superior to other organic semiconductors. These electrical properties have spurred research directed at modifying graphene for use in a variety of electronic, optoelectronic, and sensor technologies.[1,6]

In its pristine state, graphene is metallic.[5] Although graphene may be useful as a conductor, much of the current interest is in utilizing it in a semiconducting form. Therefore, introduction and control of the bandgap is crucial. For example, substitution of carbon atoms in the graphene lattice with atoms such as nitrogen has been shown to open a bandgap.[7,8] In addition, the substrate-induced band gap opening[9] and lateral confinement of charge carriers to a quasi-one-dimensional (1D) have been shown to create an energy gap near the charge neutrality point.[10]

A second and equally important challenge is to develop methods for controllably doping graphene to allow for adjustment of the work function of graphene.[11] Doping of graphene has been achieved primarily through electrostatic gating,[12] through chemical interactions,[13] and through intercalation.[11,14,15] Replacement of carbon atoms in the graphene lattice has also been shown to modulate the carrier types and concentrations in the material to allow for p- and n-type doping, and fabrication of field effect transistors (FETs) based on such substitutionally doped graphene has been achieved.[11] N-doped graphene has also been created through chemical vapor deposition (CVD) of graphene from carbonaceous precursors containing ammonia (NH_3) as a nitrogen-doping source during the deposition.[16] Similar results have also been achieved using pyridine as both the carbon and nitrogen source for CVD of graphene.[17] Most graphene samples obtained in these ways are composed of multilayer films with significant numbers of defects that reduce carrier mobilities significantly. N^+ ion irradiation of graphene followed by annealing in ammonia and nitrogen environments has also been used to modulate doping concentration in graphene flakes.[18] Alternatively, exposure of graphene to ammonia plasma has been shown to produce n-type doping.[19] In both studies where post-treatment of graphene in nitrogen containing environments was used, the result has been relatively high defect levels in the doped graphene. Therefore, due to both the complexity and the lack of control of some of these doping processes, along with the resulting high defect levels reported for many of these doping techniques, this study has focused on developing a low temperature, scalable technique for doping graphene with minimal introduction of defects.

It is well-known that the properties of graphene are sensitive to the surfaces and materials with which graphene is in contact. It has been shown that adsorbates on the graphene surface can act as dopants.[20,21] A common example is that adventitious oxygen can serve as a strong p-type dopant.[22,23] Charge transfer from such adsorbates has been used to fabricate p–n

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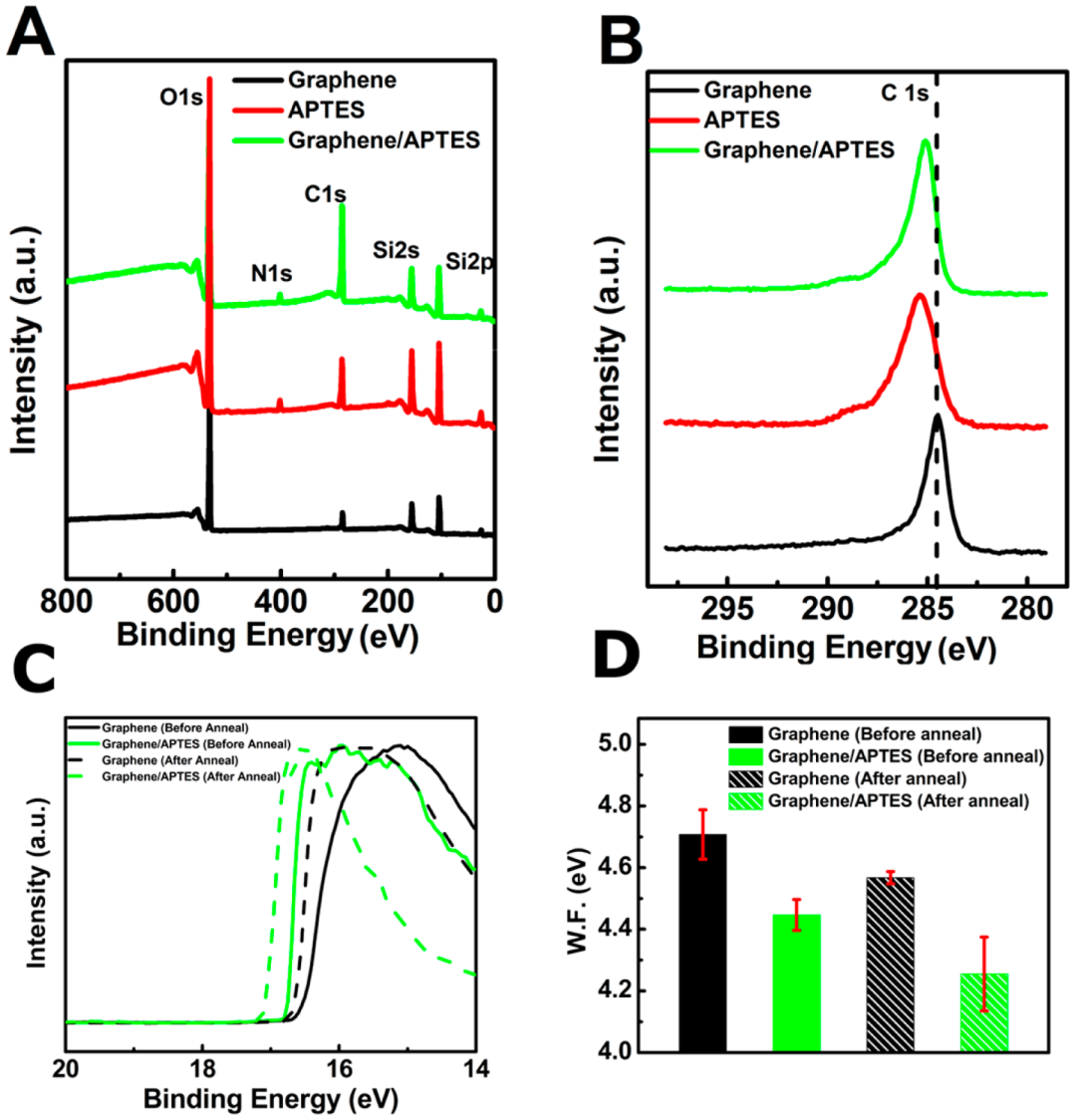

Figure 1. XPS spectra representing a (A) survey scan and the (B) C1s binding energy region for three types of samples: (black line) graphene on SiO_2, (red line) APTES layer on SiO_2, (green line) graphene on APTES coated SiO_2. (C) UPS spectra for Graphene (black) and Graphene/APTES (green), before and after anneal. (D) UPS-determined work functions. All data were normalized to the largest intensity within each spectrum.

junctions,[24−26] but the position of such junctions has been essentially random, and the dopant concentrations have not been well controlled. While such adsorbate−surface interactions make graphene potentially attractive as a sensor platform, such methods are less suitable for doping graphene in devices because of the difficulty in controlling the doping and the general lack of stability of such adsorbate layers. Surface interactions of graphene monolayers with self-assembled monolayers (SAMs) on SiO_2 substrates have also been recently studied.[27−31] While it has been observed that such monolayers can dope graphene, there has thus far been no implementation and use of SAMs to controllably dope and form p−n junctions in graphene. Most of the studies reported so far on formation of controlled p−n junctions have instead used multiple gates or electrostatic substrate engineering.[12,32−35]

In the work reported here, a facile and low temperature approach to fabricate p−n junctions on large area CVD-grown graphene has been utilized to build simple graphene FET devices containing p−n junctions in their channel. Standard lithographic methods were used to pattern a graphene FET channel containing a thin layer of aminopropyltriethoxysilane (APTES) in selected regions of the channel. Early studies suggest that amine groups can donate their lone pairs of electrons to graphene, increasing the electron carrier density and inducing n-doping in graphene.[28,30,36−38] In the process presented in this work, the intrinsically p-doped CVD graphene obtained as a result of the particular transfer process[20] utilized to deposit graphene onto the FET devices provides the basis for the p-doping required to form a p−n junction in combination with APTES layers. Upon heating the device under an inert atmosphere, the intrinsically p-doped graphene is dedoped in a controlled manner, resulting in a dopant concentration profile that leads to formation of a p−n junction. X-ray photoelectron spectroscopy (XPS) and micro-Raman spectroscopy studies confirm that the doped graphene is defect-free and that the dopant concentrations are modulated by the APTES concentration on the substrate as well as the concentration of the adsorbed molecules and atmospheric dopants on the graphene. To the best of our knowledge, this is the first time that SAMs have been used to fabricate a p−n junction that

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allows an overall control of the dopants in the junction. In addition, since the dopant layer is prefabricated and prepatterned before transfer of the graphene to the device substrate, the graphene is never subsequently exposed to photoresist and other or treatments that would otherwise be required to fabricate dopant profiles, thus allowing for control of the graphene electrical properties.

2. EXPERIMENTAL SECTION

Back-gated CVD graphene field effect transistors were fabricated using standard lithography and metallization techniques in conjunction with a solution-based self-assembled monolayer coating technique and a solution based transfer of CVD grown graphene. A highly p-doped Si wafer was used as a gate, with a 300 nm thick thermally grown silicon dioxide layer as the gate dielectric. For the APTES layer deposition, the substrate was first cleaned and pretreated by UV ozone for 15 min in order to produce a hydroxyl-terminated substrate, known to react efficiently with silane-coupling agents such as APTES. The substrate was immediately immersed in a 1% (v/v) solution of APTES in anhydrous toluene for 3 h. The substrate was removed, sonicated for 15 min in pure toluene, and dried under flowing nitrogen. Deposition was confirmed by contact angle measurements using a VCA 2000 goniometry system, by X-ray photoelectron spectroscopy (XPS), and by XPS mapping acquired using a Thermo K-Alpha XPS (Thermoscientific) operating under ultrahigh vacuum conditions with an Al Kα microfocused monochromator. For work function measurements, ultraviolet photoelectron spectroscopy, (UPS) was performed in a Kratos AxisDLD Ultra spectrometer (using He I excitation source) at base pressure 10^{-8} Torr with the Fermi energy (E_F) calibrated using an atomically clean silver sample. All samples were in electronic equilibrium with the spectrometer via a metallic clip on the graphene and characterizations were performed at normal takeoff angle (90° relative to detector).

The SAM-coated surface contained a high density of molecules that predominantly existed as free amines (i.e., non-hydrogen bonded) as characterized by X-ray photoelectron spectroscopy (XPS).[39,40] The APTES coated surface had a measured contact angle with deionized (DI) water of ~60°,[41] as compared to <10° contact angle measured immediately after the UV ozone cleaning treatment, indicative of coupling of the APTES monolayer to the surface. Finally, CVD grown graphene was transferred on top of the premade FET device structures containing either patterned APTES coated channels (i.e., ones not fully covered in APTES due to prepatterning of the channel with photoresist prior to APTES deposition) or fully APTES coated channels. The devices were immediately transferred to a nitrogen-purged glovebox. In addition to the FET devices, two types of control samples were also fabricated for collection of reference of XPS and UPS data and Raman spectra. One control sample consisted of CVD graphene transferred onto the cleaned SiO_2-coated silicon substrate containing no APTES, and one control sample contained an unpatterned, continuous APTES film.

CVD graphene was prepared following standard literature procedures.[42] Graphene was synthesized on 25 μm thick Cu foil (Alfa Aesar, item no. 14482, cut to 1 in by 1 in squares) in a low pressure $Ar/H_2/CH_4$ environment at 1000 °C.[42] PMMA (MicroChem 950 PMMA series) was then spun cast from an organic solution (9% solution in anisole, spin coated at 1500 rpm for 1 min) onto the as-grown graphene coated Cu samples and baked (180 °C for 5 to 10 min) to form an approximately 500 nm thick film that served as an auxiliary support material for handling and transferring the graphene films. The Cu foil was treated overnight with a 30 wt % $FeCl_3$ aqueous solution to completely remove copper. The resulting bilayer PMMA-graphene samples were treated with 10 wt % HCl solution for 10 min, followed by deionized (DI) water several times to remove bound contaminants. Raman spectroscopy using a 532 nm laser excitation wavelength was performed in order to verify the presence of graphene and characterize its quality.

3. RESULTS AND DISCUSSION

Figure 1a shows the XPS survey spectra for (1) the APTES-treated graphene FET devices in areas containing the APTES layer (labeled "Graphene/APTES"), (2) graphene FET devices in regions not containing the APTES layer (labeled "Graphene"), and (3) a control sample containing only the APTES layer on an SiO_2 coated silicon substrate (labeled "APTES"). These XPS survey scan spectra were collected over the binding energy (B.E.) range from 0 to 800 eV with a step size of 1 eV and a spot size of 400 μm. The clear presence of the N1s peak in Figure 1a for the Graphene/APTES and APTES samples (and lack of such a peak in the Graphene sample) supports the conclusion that the APTES SAMs were successfully deposited onto selected regions of the SiO_2 substrate in these samples. The N1s high resolution spectrum (see Supporting Information) for regions containing APTES can be deconvoluted and fit with two peaks centered at 400 eV (representing 77% of the total N1s peak area) and 401.9 eV (representing 23% of the total N1s peak area), which can be assigned to free amine ($-NH_2$) and either a protonated ($-NH_3^+$) or hydrogen-bonded amine, respectively.[40,43] The small amount of the nitrogen XPS signal assigned to the peak at 401.9 eV is likely due to protonated amine that results from the graphene transfer process (e.g., from exposure to acid). Figure 1b shows the chemical shifts in the high resolution C1s spectra for (1) regions of the FET device sample where graphene exists with no underlying APTES layer (black), (2) regions of the FET device sample where the graphene exists with an underlying APTES layer (red), and (3) a control sample with only the APTES layer deposited onto a silicon dioxide coated silicon substrate (green). We observe that for the APTES control sample the C1s peak maximum occurs with a binding energy of 285.3 eV. The shift in the C1s peak binding energy in the case of the APTES layer away from that for simple hydrocarbons (i.e., simple hydrocarbon C1s peak locations are approximately 284.5 eV) is attributed to the inductive effect of N atoms present in the APTES layer,[44] in accord with previously reported data.[29] The C1s peak for graphene on the oxide surface, at a binding energy of 284.5 eV, is typical of graphene. The C1s peak in the graphene samples deposited onto the APTES coated oxide films (Graphene/APTES) reaches its maximum at a binding energy of 285.1 eV and appears to be the result of the superposition of the graphene and APTES C1s XPS spectra.

Figure 1c shows the UPS spectra for (1) Graphene and (2) Graphene/APTES, before and after annealing at 200 °C for 4 h. The secondary electron edge occurs at the binding energy corresponding to the deepest of the energy levels that can be excited with the radiation employed. Hence, the work function Φ (energy difference between the Fermi and vacuum level) can be calculated from eq 1,[45]

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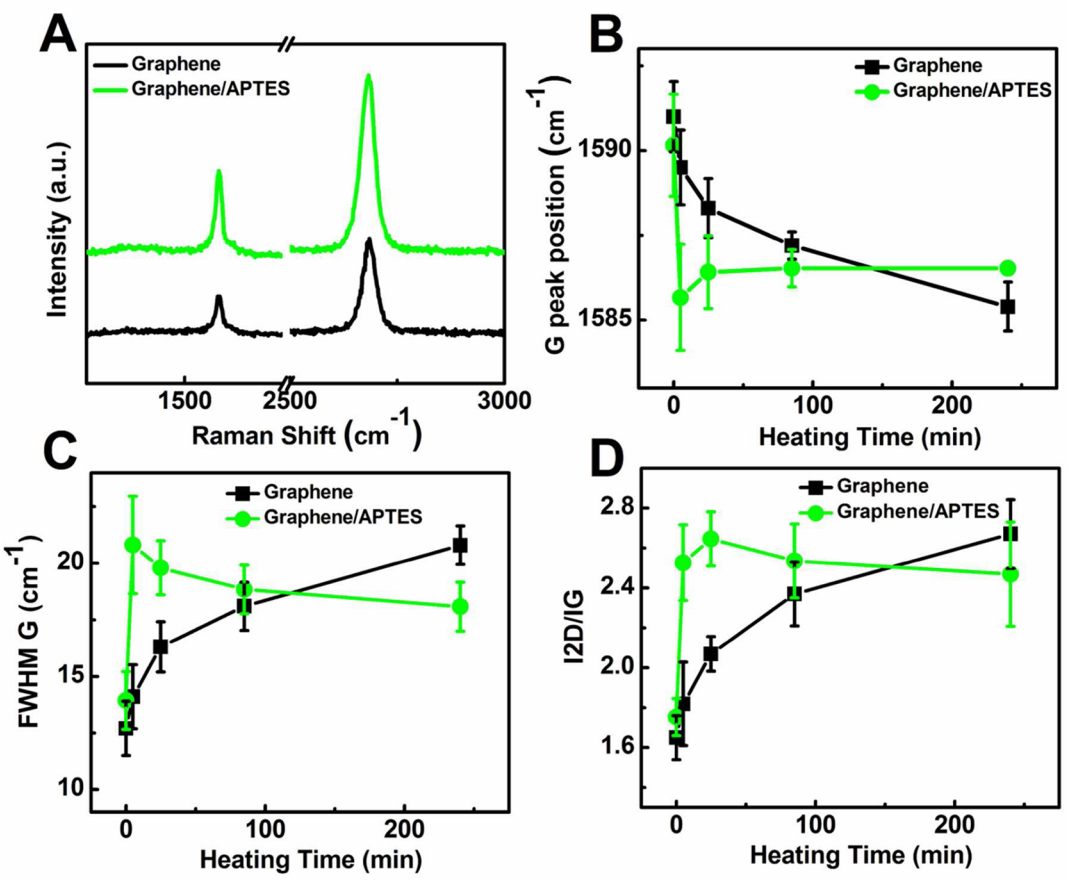

Figure 2. (A) Full Raman spectra for two samples: (black line) graphene on SiO_2 and (green line) graphene on APTES coated SiO_2. (B) G band peak position for the samples shown in 2A as a function of heating time at 200 °C. (C) fwhm of the G band for the samples shown in 2A as a function of heating time at 200 °C. (D) Ratio of 2D vs G band peak intensity for the samples shown in 2A as a function of heating time at 200 °C.

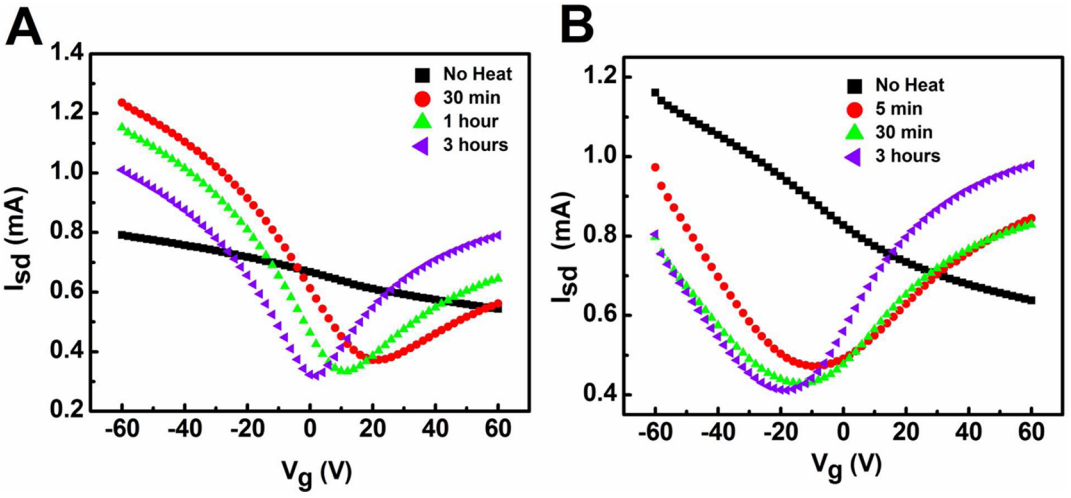

Figure 3. Source−drain current versus gate voltage for different device heating times at 200 °C for simple graphene FET devices fabricated using a simple (A) SiO_2 gate dielectric and (B) an APTES coated gate dielectric.

$$\Phi = 21.22 - BE_{SEE} \quad (1)$$

where BE_{SEE} is the binding energy at the secondary electron cutoff. The work function of graphene and graphene/APTES were determined to be 4.71 ± 0.08 eV and 4.45 ± 0.05 eV before anneal, and 4.57 ± 0.02 eV and 4.26 ± 0.12 eV after anneal, respectively. The change in the work function after anneal is attributed to the removal of external doping from impurities that can be incorporated into the graphene film during the synthesis and transfer process.[20,46] The work function of the graphene/APTES sample is ∼0.31 ± 0.12 eV lower than that of the graphene sample. This has been attributed to the lone pair electrons in the nitrogen in the amine SAMs, given that in the case of NH_3 molecules, DFT calculations have shown that there is a small charge transfer to the graphene,[47] which would explain the raising of the Fermi

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level from the Dirac point (n-doping).[29,36,48] This doping is further supported by Raman spectroscopy and electrical data discussed later (see Figures 2 and 3).

Raman spectroscopy and microscopy measurements (Horiba HR800 μRaman system) were also used to characterize the resulting graphene and graphene devices. Raman spectroscopy was utilized to investigate the quality of the graphene and its doping state by examining the D, G, and 2D bands and their positions. All spectra were excited with visible (532 nm) laser light and collected in a backscattering configuration with a laser power below 0.5 mW to reduce laser-induced heating.[21] A 50× objective lens was used to focus the laser on the graphene samples during the Raman measurements. The samples were placed inside an environmentally controlled microscope stage with heating, vacuum, and gas delivery capability (Linkam TS 1500) for in situ Raman measurements. The thermal stage was mounted onto an $X-Y-Z$ micropositioning stage to control focusing and the measurement position. A quartz window was used to allow optical access to the sample while a vacuum pump was used to evacuate the sample chamber to a pressure of ∼1 mTorr. The drift of the laser spot on the graphene due to thermal expansion was minimized before all measurements. The sample was heated to 200 °C and held at that temperature 5−90 min to allow for desorption of atmospheric adsorbed p-dopants such as oxygen and water. Raman spectra were acquired at multiple locations before and after heating and cooling to verify reproducibility. The Raman peaks corresponding to the D, G, and 2D Raman peaks in graphene were fit with Gauss−Lorentzian curve fits to determine their peak position, line width, and intensity. The as-grown graphene films utilized in this work and the graphene transferred onto the APTES layers all showed prominent graphitic (G and 2D) bands with no detectable defect peak (D) (see Figure 2a, full spectra). The high 2D over G band intensity ratio I_{2D}/I_G and low full width at half-maximum (fwhm) of the 2D band are indicative of a monolayer graphene film.[42] A critical observation is that no appearance of or increase in the D band was observed during any of the transfer or annealing steps. This indicates that successful doping, as will be shown later, of the graphene monolayer without damage to the carbon lattice structure was achieved.[29,49]

Figure 2b−d shows the G band position, the B band full width at half-maximum (fwhm), and the 2D to G band intensity ratio (I_{2D}/I_G) as a function of annealing time for both graphene transferred onto a surface region not containing APTES layer and a surface region containing the APTES layer. For graphene transferred onto APTES, the largest value of the G peak position (∼1590.2 cm^{-1}), the smallest value of full width half-maximum of the G peak (fwhm ∼36.1 cm^{-1}), and the smallest value of the I_{2D}/I_G (∼1.8) ratio were all measured before thermal annealing at 200 °C. After annealing for 5 min at 200 °C, the smallest value for the G peak position (∼1585.7 cm^{-1}), the largest G peak fwhm (∼21.1 cm^{-1}), and the largest I_{2D}/I_G ratio (∼2.5) were all characteristic of dedoped graphene.[21] Longer heat treatments at 200 °C resulted in an increase in the G peak position (∼1586.5 cm^{-1}), a decrease in the fwhm (G) (∼19 cm^{-1}), and a decrease in the I_{2D}/I_G ratio (∼2.4). These results are in agreement with the observations by Ferrari and co-workers that implicate n-doping of the graphene monolayer.[50] For samples transferred onto a substrate region without APTES, a decrease in the G peak position (from 1591 to 1588 cm^{-1}) and a broadening of the G peak (fwhm increased from 18 to 23 cm^{-1}) were observed, indicative that dedoping of the graphene has occurred due to thermal desorption of adsorbed dopants on the graphene surface.[50] (see Figure 2b)

Electrical transport properties in graphene FET devices were made in three configurations: (1) FET devices with graphene transferred directly onto SiO_2 coated channels without APTES surface treatment, (2) FET devices with graphene transferred directly onto SiO_2 coated channels covered completely with the APTES surface treatment, and (3) FET devices with graphene transferred directly onto SiO_2 coated channels partially coated in a pattern-wise manner with APTES. Electrical measurements, including $I-V$ curves, were made using a probe station configured with a HP 4156 semiconductor parameter analyzer maintained under an inert atmosphere. Measurements were performed on both as-made devices and after heating in the inert atmosphere to verify both the thermal desorption induced dedoping of the graphene and n-type doping of the graphene in the presence of APTES.

All devices, both with and without APTES, demonstrated p-doped characteristics in their as-made state, due presumably to adsorbed species on the graphene surface resulting from the CVD graphene transfer process [see Figure 3a,b].[49,51,52] As the devices were annealed at 200 °C under the inert nitrogen environment, adsorbed p-dopants were removed, leading to pristine graphene with a charge neutrality point at approximately zero volts.[46,51] Attempts were also made to dedope the devices in high-vacuum (10^{-8} Torr) combined with in situ electrical transport measurements (for up to 7 days), but no significant dedoping or shift of the neutrality point was observed in these cases (see Supporting Information). For graphene FET devices made using APTES coating the complete FET channel, as the sample is heated at 200 °C, the charge neutrality point is observed to gradually shift to lower voltages with increasing annealing time. For the APTES treated devices, the n-type doping characteristics were observed to stabilize after approximately 3 h of heat treatment at 200 °C, with the charge neutrality point (CNP) stabilizing at ca. −26 V. The electron concentration (n) of the APTES-treated graphene after annealing was approximately 2×10^{12} cm^{-2}, as calculated using eq 2,[46,53]

$$n = C_g V_{np}/e \tag{2}$$

where C_g = 115 aF/μm^2,[54] e is the charge of the electron, and V_{np} is the voltage at the charge neutrality point. The electron concentration (n) is related to the energy position of the Dirac point by[55]

$$E_D = \hbar v_F (\pi n)^{-1/2} \tag{3}$$

where v_F is the Fermi velocity of graphene (1.1×10^{-6} ms^{-1}).[27] The calculated energy position of the Dirac point is ∼0.2 eV after anneal, which is close to the shift of the graphene work function from the control (∼0.3 ± 0.1 eV, Figure 1c).

The field-effect mobility for both of the devices was ∼434 ± 100 $cm^2/(V\ s)$ (hole and electron mobility), extracted using[6]

$$\mu = L_{ch} g_m / W_{ch} V_{ds} C_{ox} \tag{4}$$

where μ= mobility, L_{ch}= 2000 μm, g_m= dI_D/dV_{GS}, W_{ch}= 50 μm, V_{DS}= 0.1 V and C_g = 115 aF/μm^2. This result indicates that the APTES layer was able to dope the graphene in the FET device without otherwise affecting or degrading its mobility as compared to devices made without the doping layer. This is consistent with previous studies that have indicated that contact

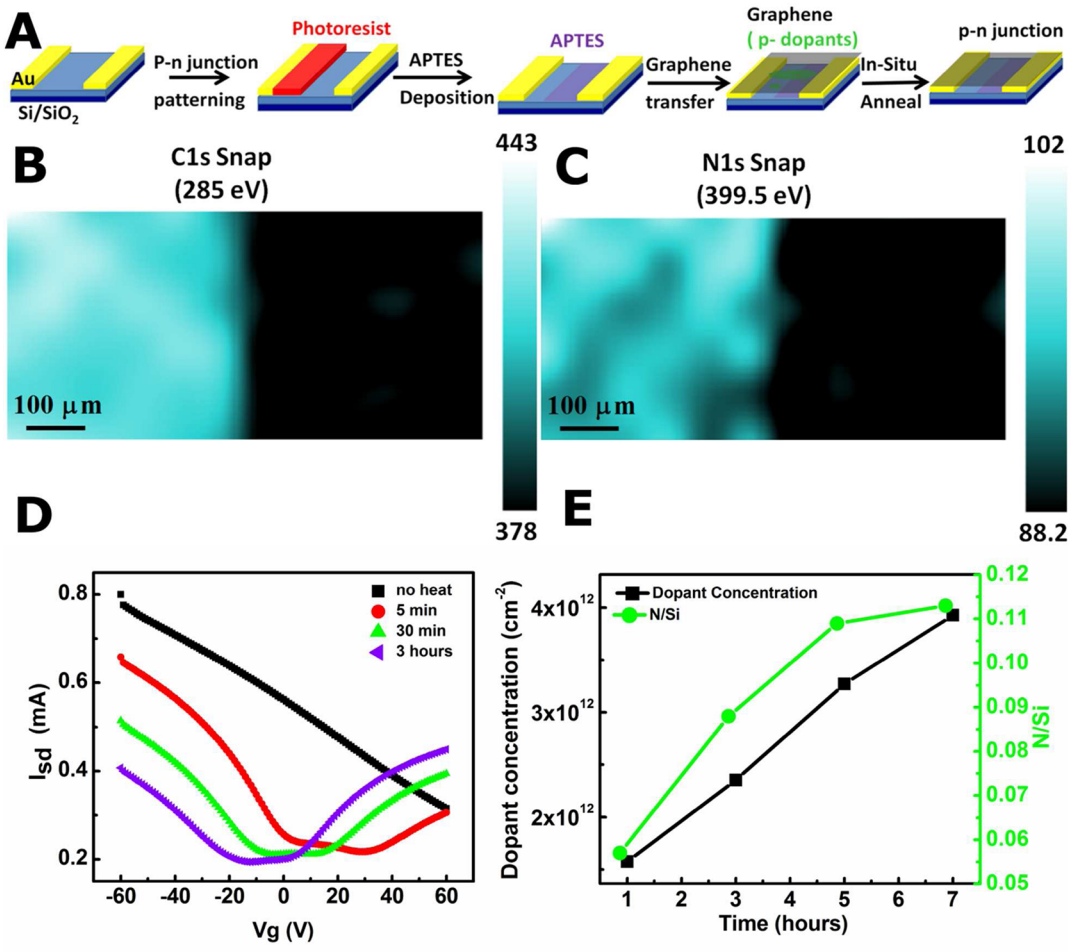

Figure 4. (A) Schematic showing the process used to fabricate the graphene p−n junction. XPS mapping of the graphene p−n junction for the (B) C1s intensity at a binding energy of ∼285 eV (C) N 1s intensity at a binding energy of 399.9 eV. (D) Source−drain current versus gate voltage as a function of heating times at 200 °C for a graphene p−n junction. (E) Dopant concentration and nitrogen/silicon (N/Si) ratio versus APTES deposition time.

of graphene with self-assembled monolayers has not significantly affected their mobilities as compared to graphene in contact with substrates not containing the SAMs.[13,28,30]

Back-gated graphene-based p−n junction with patterned p−n regions in the FET channel were fabricated and measured following the same basic process described above. Figure 4a illustrates the fabrication steps involved in making the patterned p−n junctions in the FET channel devices. After lithography and deposition processes (i.e., typical lift-off procedures) were used to form the gold electrodes on the 300 nm thick SiO_2 gate dielectric films on highly p-doped silicon wafers, half of each of the channels in the FET devices were patterned with photoresist and hard baked. The device samples were then treated with APTES using the same solution processing sequence described earlier to deposit APTES in the half of each device channel that was not protected by hard-baked photoresist. The photoresist was removed by placing the devices in *N*-methylpyrrolidone (NMP) for 1 h, followed by further sonication in acetone and inspection by optical microscopy to ensure removal of all photoresist.

The resulting patterned APTES layers were verified by XPS mapping as illustrated in Figure 4b. XPS mapping was performed using a 30 μm spot size with a step size of 28 μm, and a Gaussian smoothing algorithm was applied to the raw data. The signal associated with 399.5 eV binding energy was used for mapping the N1s spectra. The figure shows a well-defined boundary between areas of the substrate coated with the APTES layer and those without. Further analysis of the position of these boundaries with respect to the location and intensity of peaks in the XPS originating from the gold source and drain contacts confirm that the lithographic alignment was sufficient to locate these p−n junctions in the FET channels. C1s mapping using a binding energy centered at 285 eV was also performed. Again, a well-defined boundary is observed in the patterned APTES samples, with the strongest C1s signal corresponding to regions containing the strongest N1s signal as well, consistent with the formation of a well-defined patterned APTES layer.

Electrical measurements were performed on the fabricated CVD graphene devices containing the patterned APTES in the device channels by probing the devices under inert atmosphere using a method similar to that described previously. As expected, as-made devices exhibited a heavily doped p-type characteristic (Figure 4 c) due presumably to doping from adsorbed species. The two expected current minima region for the devices in the as-made state were located at sufficiently large positive gate potentials to preclude measurement without breakdown of the device dielectric. After annealing at 200 °C for only 5 min, two minima in the $I_{sd}-V_g$ data were clearly observed, corresponding to two Dirac points as a result of

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desorption of p-dopants. For V_g larger than approximately +35 V in this device, the device channel was effectively in a n/n+ doping configuration where both regions of the channel were p-doped, but the region of the channel that does not contain the APTES layer was more heavily p-doped. For V_g of approximately 0 to +35 V, the formation of a p−n junction in the device channel was observed. For V_g less than 0 V, the device channel existed in a p+/p doping configuration where the regions of the channel containing the APTES layer were more heavily n-doped. After 30 min of annealing at 200 °C, the device channel was n/n+ doped for V_g larger than +15 V, p−n doped for V_g between −10 V and +15 V, and p/p+ doped for V_g less than −10 V. These behaved roughly symmetrically in terms of electrical response around V_g = 0 V. Further annealing led to additional shifts of the V_g range over which a p−n junction doping profile existed in the device channel to more negative V_g. It was also possible during these measurements to demonstrate the unique ambipolar character of the devices. Switching of the source−drain bias voltage from positive to negative values showed no rectifying behavior as would be characteristic of an ambipolar device.[12,56]

In addition to using this strategy of patterning the amine layer to introduce controlled modulation of the doping profile in the device channel, it is also of course possible to modulate the amount of free amine on the substrate by changing the time or solution concentration conditions used to deposit the amine. This modulation of the amount of APTES on the dielectric surface can in turn be used to modulate the doping level in the devices. To demonstrate this, the APTES deposition time was varied between 1 and 7 h for devices made with the unpatterend APTES layer covering the entire device channel. Figure 4 shows the carrier concentration measured in the graphene devices along with the nitrogen to silicon ratio (N/Si) obtained by XPS in each of these samples as a function of APTES deposition time. Clearly the carrier concentration is observed to scale roughly with APTES deposition time over the range of APTES deposition times measured. One would expect this behavior to saturate once a sufficiently dense and thick enough APTES layer is formed such that no further electronic influence on the graphene film is created by further deposition of APTES. Carrier concentrations in excess of 4.5×10^{12} cm^{-2} were observed in the devices measured, corresponding to a CNP change above −60 V (see Supporting Information, Figure 2). This ability to control the n-doping characteristics of the device surface, that is, through modulation of the density of APTES deposited (e.g., by controlling deposition time or solution concentration) on the gate dielectric, can be easily combined with the patterned p−n junction fabrication techniques to allow for full control of the position of the charge neutrality points in the $I-V$ characteristics of the resulting FET devices. This unique p−n junction behavior of graphene, in contrast with the traditional rectifying behavior of conventional semiconductors, allows the development of graphene-based bipolar devices which have been demonstrated to display new and exciting phenomena such as Klein tunneling,[32,33,35] and produce lensing effects for coherent electrons, that is, so-called Veselago lensing.[57] Our simple method for producing patterned doping profiles in graphene films and devices facilitates the study of such phenomena since it allows precise and independent control over the characteristics of the FET $I-V$ curves as compared to the more limited control possible with electrostatic substrate engineering,[12] and other fabrication techniques.[25,26,33,35,58]

4. CONCLUSIONS

The use of a self-assembled covalent APTES monolayer has been demostrated to n-dope graphene, controlling the resulting doping level in graphene FET devices depending upon the amount of APTES deposited onto the FET gate dielectric surface. Production of FET devices with patterned p- and n-doped regions through lithographic patterning of such APTES layers using the combination of control of APTES deposition and patterning to tune the $I-V$ characteristics of graphene FET devices was done. It has also been shown that use of such APTES doping schemes does not degrade the resulting graphene electronic properties as has been problematic in previously reported doping procedures due to introduction of defects into the graphene layer. Overall, the methods described here allow for facile, controllable, and low temperature fabrication of graphene p−n junctions.

■ ASSOCIATED CONTENT

Supporting Information

N1s peak deconvolution, IV characteristic for graphene/APTES device as a function of APTES deposition time, and IV characteristics for a graphene/APTES FET device as a function of pump down time. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

#J.B. and H.S. contributed equally to this work.

Notes

The authors declare no competing financial interest.

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